IN THE CLAIMS

Please substitute the following amended claims for corresponding claims previously presented. A copy of the amended claims showing current revisions is attached.

3. A data processor according to claim 1 wherein the means for independently addressing the two types of unit cells addresses each type of unit cell by applying to the whole array the state transformation signal in the form of a physical stimulus to which unit cells of the other type are substantially inert.

4. A data processor according to claim 1 wherein the array is one dimensional, consisting of a line of unit cells of alternating type.

6. A data processor according to claim 1 wherein data bits are represented on the array as patterns of said first and second states, each data bit being represented by a pattern of states formed by a plurality of adjacent unit cells.

7. A data processor according to claim 1 wherein each data bit is represented by a pattern of states formed by four adjacent unit cells.

9. A data processor according to claim 1 further comprising at least one of: first means for simultaneously addressing all unit cells of the array with a state transformation signal to which all the unit cells respond; second means for

simultaneously addressing all unit cells of the array with a 15 state transformation signal to which the unit cells respond in dependence on the states of their nearest neighbours;

third means for addressing all unit cells of one of said different types in the array with a state transformation signal to which all the unit cells of said onetype respond.

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10. A data processor according to claim 1 wherein the state transformation switches the state of the unit cell between said first and second distinguishable states.

11. A data processor according to claim 1 further comprising loading means for loading data onto the array by applying a first state transformation to a unit cell on the edge of the array to set it into a desired state and a second state transformation to move the data to a neighbouring unit cell within the array by transforming said neighbouring unit cell into the same state.

13. A data processor according to claim 11 wherein the loading means is operable to load a control unit onto the array, the control unit comprising a predetermined pattern of states of a plurality of adjacent unit cells.

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16. A data processor according to claim 13, wherein there are a plurality of control units each having associated with it a set of states constituting a label such that each of

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said plurality of control units may be independently manipulated by a computational process involving each control unit and its label.

18. A data processor according to claim 16 wherein the label comprises a plurality of unit cells adjacent the control unit.

19. A data processor according to claim 16 wherein each of said plurality of control units also has associated with it a plurality of adjacent unit cells set into a predetermined state.

20. A data processor according to claim 16 wherein pairs of 10 adjacent control units are mutually separated by a plurality of data bits.

21. A data processor according to claim 16 wherein each region of the data processor hitherto containing a single control unit and its associated label bits is extended to include additional control units and labels so as to provide parallel computation within that region.

22. A data processor according to claim 16 wherein a plurality of different transformations are applicable to the control units corresponding to different subsequent operations on the data bits.

23. A data processor according to claim 16 wherein the labels and auxiliary bits associated with each control unit are represented by quantum systems in a quantum superposition of states, whereby the control units may be in a superposition of an enabled and disabled state.

24. A data processor according to claim 1 wherein said unit cells are Boolean variables in an array stored in the memory of a computer.

25. A data processor according to any one of claim 1 wherein the unit cells are quantum systems and said distinguishable states are different eigenstates of the system such that each unit cell can be in a quantum superposition of the distinguishable states.

26. A data processor according to claim 25 wherein the state transformation is a unitary transform.

27. A data processor according to claim 26 wherein the quantum systems are non-zero-spin nuclei of a molecule, said distinguishable states being different spin states, said state transformations being effected by illumination of the array with electromagnetic radiation of a frequency selected to flip the spin of the unit cells to be addressed.

28. A data processor according to claim 26 wherein the quantum systems are non-zero-spin nuclei of donor impurity atoms in a semiconductor.

29. A data processor according to claim 23 wherein the unit cells are quantum systems and said distinguishable states are different eigenstates of the system such that each unit cell can be in a quantum superposition of the distinguishable states.

Please add the following new claims 30-32:

30. (NEW) A data processor according to claim 29 wherein the state transformation is a unitary transform.

31. (NEW) A data processor according to claim 30 wherein the quantum systems are non-zero-spin nuclei of a molecule, said distinguishable states being different spin states, said state transformations being effected by illumination of the array with electromagnetic radiation of a frequency selected to flip the spin of the unit cells to be addressed.

32. (NEW) A data processor according to claim 30 wherein the quantum systems are non-zero-spin nuclei of donor impurity atoms in a semiconductor.